

# Suspended Highly-efficient On-chip Phased Array Antenna at 60 GHz

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**Abstract**—This paper presents an on-chip millimeter-wave (mmW) phased array antenna for the next-generation wireless systems. Current silicon-based mmW antennas exhibit low radiation efficiency (~5-10%) due to lossy substrate. The proposed on-chip antenna array can achieve radiation efficiency >80% using micro-electro-mechanical systems (MEMS) processes. By suspending the radiating antennas, a low- $\epsilon_r$  substrate of air is formed instead of a lossy silicon substrate. The designed 5×5 (element) array is well matched at 60 GHz covering a bandwidth of 2 GHz with at least -10 dB return loss. The peak realized gain for this array is 19.7 dBi with the side-lobe level of -13 dB. Moreover, the maximum scanning volume of the designed antenna is  $\pm 45^\circ$  in  $H$  plane and  $\pm 48^\circ$  in  $E$  plane. As an on-chip antenna, the proposed array can be monolithically integrated on a silicon substrate. Moreover, unlike other arrays, it satisfies high realized gain and moderate scanning volume in both  $E$  and  $H$  planes, making it desirable for the next-generation communication systems.

**Keywords**— *Suspended; 60 GHz; Phased array; Millimeter-wave, On-chip; Antenna.*

## I. INTRODUCTION

As the cellular data traffic rapidly increases, the future wireless communication systems are expected to require higher data rates [1]. The 60 GHz band has emerged as one of the candidates due to available 7 GHz unlicensed spectrum (57-64 GHz) targeting short-range communication. However, due to large path loss at 60 GHz [2], innovations are needed in several areas including efficiency and steering capability.

The major problems of current on-chip antennas-utilized for direct on-chip integration-is low radiation efficiency (5-10%) and consequently low realized gain because most of power radiates into the substrate [2-3]. This is due to the fact that the antenna radiates into the substrate [2-3]. Currently there are several approaches to increase the efficiency of on-chip antennas. For example, a thin layer of silicon dioxide ( $\text{SiO}_2$ ) is employed to separate radiating element from the ground. It is important to note that the height of this  $\text{SiO}_2$  layer is limited due to fabrication restraints, thus decreasing the radiation resistance. As a result, the efficiency is small.

This paper presents a novel architecture to achieve >80% efficiency using MEMS suspension. By suspending the patch antenna away from the silicon substrate, the effective dielectric constant is decreased, thus reducing the losses due to dielectric, conductive, and surface wave modes. Furthermore, the capacitive feeding scheme is adopted for the ease of fabrication and monolithic integration with T/R modules. In addition, we

have improved our previous work [4-5] by optimizing feeding network using coplanar waveguide (CPW) feeding line rather than microstrip line feeding network, thus reducing the radiation loss and crosstalk. Furthermore, it simplifies fabrication and monolithic integration by eliminating the thick  $\text{SiO}_2$  layer. In Section II, the design of antenna architecture is presented. The fabrication of the phased array antenna is analyzed in Section III. Finally, the scanning range in both  $E$  and  $H$  planes are analyzed and the impedance bandwidth is discussed in Section IV.

## II. ANTENNA DESIGN

### A. Unit-cell design

The unit-cell of on-chip phased array is illustrated in Fig.1 [6]. The proposed architecture elevates patch antennas away from the lossy silicon substrate, which is achieved by SU-8 epoxy posts. As can be seen, a number of SU-8 posts support the radiating patch 60  $\mu\text{m}$  above the ground. As an epoxy-based negative photoresist, SU-8 polymer is used as vertical posts due to its high-aspect-ratio nature [7]. Consequently, an air substrate of low- $\epsilon_r$  is created to replace the lossy and high- $\epsilon_r$ .

Moreover, the radiating patch is fed using capacitive feeding cap, which is supported by the 40- $\mu\text{m}$ -thick probe, fabricated by metallization of inner SU-8 post. For capacitive coupling, the distance between the radiating patch and feeding cap determines the suitable mode for patch antenna, which is also optimized for impedance matching and efficiency improvement. Capacitive feeding simplifies the fabrication process by dividing the architecture into two wafers, which can be fabricated separately and bonded for the final design.

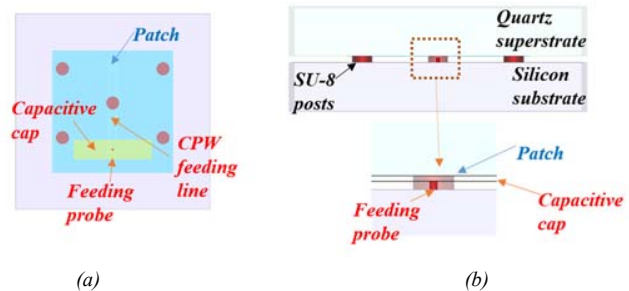


Fig.1. a) Top view and b) side view of unit-cell of proposed phased array.

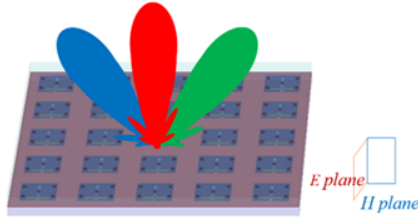


Fig.2. 3D view schematic of the proposed 5×5 array

### B. Phased Array design

As can be seen from Fig.2, the array is chosen as 5×5 (12.5 mm×12.5 mm) for ease of design and measurement. The element spacing is 2.5 mm or half the free-space wavelength at 60 GHz. In practice, each array element will be fed with a T/R module to form an active electronically scanned array.

### III. FABRICATION

The proposed antenna array is fabricated on a silicon wafer. First, the CPW feeding network is patterned using 1-μm-thick gold layer. Next, the feeding probe is patterned. Then another gold layer is patterned to form the capacitive feeding cap. In addition, the radiating patch is fabricated on a separate Quartz wafer. Then five SU-8 supporting posts are spin coated and patterned for suspension. Finally, the quartz wafer is flipped over and bonded to previous silicon wafer for the final structure.

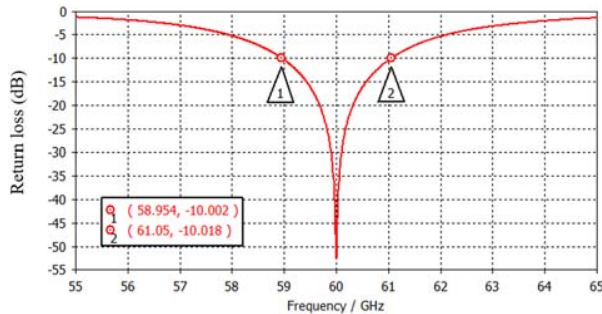


Fig.3. Simulated  $S_{11}$  of the center element of the 5×5 array at broadside scanning showing that -10 dB bandwidth is 2 GHz.

### IV. RESULTS AND CONCLUSION

As can be seen in Fig. 3, the -10 dB impedance bandwidth of the designed array is 2 GHz, which is sufficient for most 60 GHz applications. Fig. 4 presents the realized gain at  $E$  plane and  $H$  plane, respectively. As can be observed, the peak realized gain is 19.7 dBi with side-lobe level of -13 dB at broadside. Moreover, this 5×5 array is capable of  $\pm 45^\circ$  scanning in  $H$  plane

and  $\pm 48^\circ$  in  $E$  plane. As can be seen, the gain reduction is less than 5 dB for maximum scanning angle. The radiation efficiency of the phased array antenna is calculated to be 85% but hasn't experimentally verified yet. Detailed fabrication process, together with antenna scanning analysis and measurements will be presented at the conference.

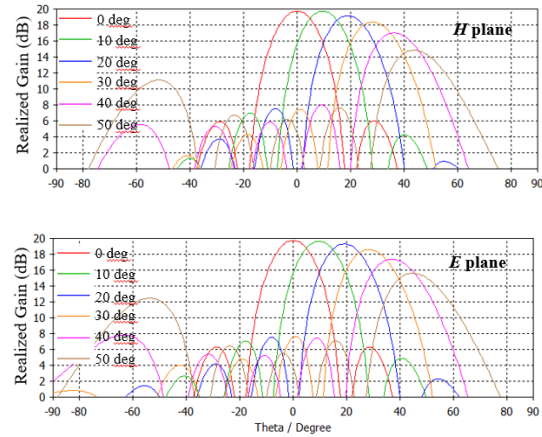


Fig.4. Simulated  $H$ -Plane (top) and  $E$ -Plane (bottom) radiation patterns (realized gain) of the 5×5 array as a function of scanning angle ( $0^\circ$  to  $50^\circ$  with  $10^\circ$  steps) at 60 GHz.

### ACKNOWLEDGMENT

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